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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,065	01/29/2004	Toshiharu Furukawa	ROC920030268US1	5663
30206	7590	05/12/2005	EXAMINER	
IBM CORPORATION			NADAV, ORI	
ROCHESTER IP LAW DEPT. 917			ART UNIT	PAPER NUMBER
3605 HIGHWAY 52 NORTH				
ROCHESTER, MN 55901-7829			2811	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	<i>S/M</i>
	10/767,065	FURUKAWA ET AL.	
	<b>Examiner</b>	Art Unit	
	ori nadav	2811	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1)  Responsive to communication(s) filed on 07 April 2005.

2a)  This action is FINAL.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

- 4)  Claim(s) 1-10 and 25-28 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-10 and 25-28 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 29 January 2004 is/are: a)  accepted or b)  objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)  All    b)  Some \* c)  None of:

  1.  Certified copies of the priority documents have been received.
  2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 01/29/04.

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_.

**DETAILED ACTION*****Election/Restrictions***

Applicant's election without traverse of claims 1-10 and 25-28 in the reply filed on 04/07/2005 is acknowledged.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification describes a gate electrode formed above a substrate and a gate dielectric interposes in between. There is no support and adequate description in the disclosure and drawings for a gate electrode projecting vertically from said substrate, as recited in claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. The claimed limitations of a gate electrode projecting vertically from said substrate, as recited in claim 1, are unclear as to how the gate electrode can project from the substrate when the gate electrode is isolated from the substrate by a gate dielectric.

The claimed limitations of at least one semiconducting nanotube extending vertically through said gate electrode between opposite first and second ends, a source electrically coupled with said first end of said at least one semiconducting nanotube; and a drain electrically coupled with said second end of said at least one semiconducting nanotube, as recited in claim 1, are unclear as to which element first and second ends refer since at least one semiconducting nanotube extending vertically through said gate electrode between opposite first and second ends of the gate electrode, whereas the source and drain regions are electrically coupled with first and second end of said at least one semiconducting nanotube.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Jin et al. (6,250,984).

Jin et al. teach in figure 9 and related text a semiconductor device structure, comprising:

a substrate 105 defining a substantially horizontal plane;

a conductive first plate 104 disposed on said substrate,

at least one nanotube 103 projecting vertically from said first plate and electrically coupled with said first plate;

a conductive second plate 100A positioned vertically above said first plate; and

a dielectric layer 101A electrically isolating said second plate from said first plate and said at least one carbon nanotube,

wherein said at least one nanotube has a conducting molecular structure,

wherein said at least one nanotube has a semiconducting molecular structure,

and

wherein said dielectric layer defines a coating that encases said at least one nanotube.

Claims 1, 4-8 and 10, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth et al. (6,858,891).

Farnworth et al. teach in figure 1 and related text a vertical semiconductor device structure, comprising:

a substrate 12 defining a substantially horizontal plane;

a gate electrode 19 projecting vertically from said substrate;

at least one semiconducting nanotube 22 extending vertically through said gate electrode between opposite first and second ends;

a gate dielectric 20 electrically insulating said at least one semiconducting nanotube from said gate electrode;

a source 17 electrically coupled with said first end of said at least one semiconducting nanotube; and

a drain 21 electrically coupled with said second end of said at least one semiconducting nanotube, an insulating layer disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode, an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane, and wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-3 and 9, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al.

Regarding claim 9, Farnworth et al. teach in figure 1 substantially the entire claimed structure, as applied to claim 1 above, except a plurality of semiconducting nanotubes extending vertically through said gate electrode. Farnworth et al. teach in figure 2 a plurality of semiconducting nanotubes 22 extending vertically through said gate electrode.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of semiconducting nanotubes extending vertically through said gate electrode in Farnworth et al.'s device in order to use the device in an practical application which requires plurality of nanotubes.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Farnworth et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722**

and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is (571) 272-1660. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is 308-0956



O.N.  
5/10/05

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PRIMARY EXAMINER  
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